

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

**Burden Hour Statement:** This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, P.O. Box 1450, Alexandria, Virginia, 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia, 22313-1450.**

Substitute for form 1449A/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Application / Conf. No.</b>	Unknown /
				<b>Filing Date</b>	February 20, 2004
				<b>First Named Inventor</b>	Kevin T. Look
				<b>Art Unit</b>	Unknown
				<b>Examiner Name</b>	Unknown
<b>Sheet</b>	2	<b>of</b>	2	<b>Attorney Docket Number</b>	X-1462-2P US

OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		HE, LEI; "Power Efficient FPGA: Circuit, Fabrics and CAD Algorithms," Presentation on February 13, 2004, 50 pages, at Xilinx, Inc. 2100 Logic Drive, San Jose, CA 95124, available from EE Department, UCLA, at <a href="http://eda.ee.ucla.edu/">http://eda.ee.ucla.edu/</a> .	
		FPGA 2004 ADVANCE PROGRAM; "ACM/SIGDA Eleventh international Symposium on Field Programmable Gate Arrays, February 22-24, 2004, 6 pages, at Monterey Beach Hotel, Monterey, California, available at <a href="http://fpga2004.ece.ubc.ca/">http://fpga2004.ece.ubc.ca/</a>	
		INUKAI, T. et al., "Boosted Gate MOS (BG MOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," 2000, pages 409-412, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
		HAMZAOGLU, F. et al., "Circuit-Level Techniques to Control Gate Leakage for sub-100nm CMOS," ISLPED, August 12-14, 2002, Pages 60-63, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
		KURODA, T., et al., "A 0.9V, 150-MHz, 1-mW, 4 mm <sup>2</sup> 2-D Discrete Cosine Transform Core Processor with Variable Threshold-Voltage (VT) Scheme, 1996, pages 1770-1779, Vol. 31, No. 11, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
		MUTOH, S. et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," August 1995, pages 847-854, Vol. 30, No. 8, available from IEEE Journal of Solid-State Circuits, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.